

REMARKS/ARGUMENTS

Applicants received the Office Action dated June 5, 2007, in which the Examiner: 1) rejected claims 1-2, 4-5, 8-13 and 15-20 under 35 U.S.C. § 102(b) as being allegedly anticipated by Duley (U.S. Pat. No. 5,526,253, hereinafter “Duley”); 2) rejected claim 3 under 35 U.S.C. § 103(a) as being allegedly unpatentable over Duley; 3) rejected claims 6 and 14 as being allegedly unpatentable over Duley in view of Chandrakasan (U.S. Pat. No. 6,967,522, hereinafter “Chandrakasan”); and 4) rejected claim 7 as being allegedly unpatentable over Duley in view of Atkinson (U.S. Pat. No. 5,991,883, hereinafter “Atkinson”). With this Response, Applicants have amended claims 1, 6, 7, 12, 16, and 18.

I. REJECTIONS UNDER U.S.C. § 102(b)

Duley is directed to a power supply. A power supply generates and supplies operating power for a load. Duley is specifically directed to a boost circuit usable with a power supply. Figure 1 of Duley shows a boost circuit 10 coupled to a power control circuit 26. Duley explains that a power supply comprises the combination of the boost circuit 10 and the power control circuit 26. Col. 5, II. 42-44. Figure 2 illustrates the power control circuit 26 provides operating voltage that is provided to one or more loads (RL_1 and RL_2). The operating voltage provided to each load is either the voltage from the battery 28 or V_{in} which is derived from AC power (e.g., wall outlet). Col. 5, II. 56-61. Components Q1, Q2, and Q3 are transistors that are turned on and off by control signals provided on their gate terminals. The control signal is V_{out} which is provided to the gate terminals by way of resistors R_9 , R_{10} , and R_{11} , respectively. The boost circuit 10 (Fig. 1) generates V_{out} by way of a voltage multiplier 14 which operates in concert with an oscillator 12. A control regulator 18 turns the oscillator on and off (standby mode) based on the magnitude of V_{out} .

Claim 1 requires that, “if an operating voltage for the system is between two thresholds, the power management logic forces the electrical load to operate in a reduced power state.” The Examiner did not clearly identify what is believed to be akin to either the claimed “electrical load” or the “operating voltage for the system.” Duley’s oscillator 12 is turned on and off based on the magnitude of V_{out} . Applicants assume that the Examiner contends that Duley’s oscillator 12 and voltage V_{out} are akin to the claimed “electrical load” and “operating voltage,” respectively. Applicants respectfully request clarification if Applicants’ understanding of the Examiner’s rejection is incorrect.

Duley’s voltage V_{out} is used to turn the transistors Q1-Q3 on and off to thereby enable operating voltage V_{in} or the battery voltage to power the load(s) RL₁ and RL₂. The voltage V_{in} is not an “operating voltage for the system.” Thus, Duley does not disclose an “operating voltage” for a system, the level of which determines whether power management logic forces the electrical load to operate in a reduced power state.

Further, one of ordinary skill in the art would not fairly consider Duley’s oscillator 12 to be an “electrical load” as claimed. Duley’s oscillator 12 is part of the power supply, specifically the boost circuit 10, and is not an electrical load. Applicants have clarified this distinction by amending claim 1 to state that the “electrical load comprises at least one of a CPU, a display, and memory.” To the extent the Examiner believes Duley’s oscillator 12 is akin to the claimed “electrical load,” the oscillator 12 certainly is not a CPU, a display, or memory.

For either or both of these reasons, claim 1 and its dependent claims are allowable over Duley. None of the other art satisfies the deficiencies of Duley. Applicants amend claims 6 and 7 per the amended language of claim 1.

Applicants amend claim 12 to clarify that the distinction of the claimed “operating voltage” over the voltage V_{out} of Duley. The voltage V_{out} of Duley is not an operating voltage “for the electrical load” as is now required by claim 12. The voltage for the loads RL₁ and RL₂ in Duley is either V_{in} or the battery voltage and Duley’s power management logic does not force the system to operate in a reduced power state when V_{in} or the battery voltage for the load is between two

voltage thresholds. Further, Duley's oscillator 12 would not fairly be considered to be an "electrical load" by one of ordinary skill in the art. None of the other art satisfies the deficiencies of Duley. For at least these reasons, claim 12 and its dependent claims are in condition for allowance.

Claim 16 has been amended to clarify that the operating voltage is an operating voltage "for a load." Duley's V_{out} is substantially different from the claimed operating voltage as explained above. Duley's operating voltage— V_{in} or the battery voltage—is not assessed to be between first and second reference voltages for purpose of causing the system to operate in a non-programmed, reduce performance mode, as is required by claim 16. None of the other art satisfies the deficiencies of Duley. For at least this reason, claim 16 and all claims dependent thereon are in condition for allowance.

Method claim 18 has been amended to require comparing an operating voltage "for a load" to first and second reference voltages, and then using the result of this comparison to require the system to operate in a less than full performance mode. As explained above, Duley has no such teaching. None of the other art satisfies the deficiencies of Duley. For at least this reason, claim 18 and all claims dependent thereon are in condition for allowance.

II. REJECTIONS UNDER U.S.C. § 103(a)

The Examiner rejected claims 3, 6, 7, and 14 as obvious over Duley and other art. Such claims depend from independent claims that have been demonstrated to be allowable over Duley. The other art of record does not satisfy the deficiencies of Duley with regard to the independent claims. Because claims 3, 6, 7, and 14 inherit the limitations of the independent claims, claims 3, 6, 7, and 14 are also in condition for allowance.

III. CONCLUSION

Applicants respectfully request reconsideration and that a timely Notice of Allowance be issued in this case. It is believed that no extensions of time or fees are required, beyond those that may otherwise be provided for in documents accompanying this paper. However, in the event that additional extensions of time are necessary to allow consideration of this paper, such extensions are

**Appl. No. 10/734,938
Amdt. dated September 5, 2007
Reply to Office Action of June 5, 2007**

hereby petitioned under 37 C.F.R. § 1.136(a), and any fees required (including fees for net addition of claims) are hereby authorized to be charged to Hewlett-Packard Development Company's Deposit Account No. 08-2025.

Respectfully submitted,

/Jonathan M. Harris/
Jonathan M. Harris
PTO Reg. No. 44,144
CONLEY ROSE, P.C.
(713) 238-8000 (Phone)
(713) 238-8008 (Fax)
ATTORNEY FOR APPLICANTS

HEWLETT-PACKARD COMPANY
Intellectual Property Administration
Legal Dept., M/S 35
P.O. Box 272400
Fort Collins, CO 80527-2400